



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Martin Ratcliffe
Serial No.: 09/855,011
Title: VIDEO HORIZONTAL AND VERTICAL VARIABLE SCALING FILTER
Filed: May 14, 2001
Attorney Docket No.: 00-323 / 1496.00121
Examiner: Rosario, D.
Art Unit: 2624

CERTIFICATE OF MAILING

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 10, 2006.

By: Jan M. Dunbar
Jan M. Dunbar

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal by an attorney either of record or acting under 37 CFR 1.34.

REMARKS

Review is requested for the following reasons:

1. The limitation in claim 1 of "wherein said address generator circuit comprises a finite state machine" is not met by the references. Specifically, the Office Action associates the presently claimed address generator circuit with the DMA device 384 in FIG. 5 of Yasuki and the presently claimed finite state machine with the State Machine 385 in FIG. 5 of Yasuki.¹ A person having an ordinary level of skill in the field of the presently claimed invention would not consider the **separate** DMA device 384 and State Machine 385 of Yasuki as meeting the limitation in claim 1 of "wherein said address generator circuit comprises a finite state machine." In particular, see the arguments presented on page 10, line 24 through page 16, line 2 in the Amendment After Final, filed March 13, 2006.

2. The Examiner has clearly made the following errors in the rejection(s).

The argument presented by the Examiner in section 2, on page 2 of the Advisory Action² that "the DMA device 384 does **comprise** the state machine 385 **because both** the DMA device 384 and

¹ See page 8 of the final Office Action mailed January 12, 2006.

² Mailed April 4, 2006.

the state machine 385 **share a common connection or bus . . .**³ does not appear to apply the proper meaning for the transitional phrase "comprises." Specifically, the use of the word "comprise" as meaning "connected to" is clearly erroneous. In particular, the words "comprises" and "comprising," in patent law, are synonymous with "including," "containing," or "characterized by."⁴ Clearly, since Yasuki shows the state machine 385 as a separate box, external to a box identifying the DMA device 384, it follows that the DMA device 384 of Yasuki does not "include" or "contain" the state machine 385 of Yasuki. Therefore, the DMA device 384 of Yasuki does not comprise the state machine 385 of Yasuki. As such, the limitation in claim 1 of "wherein said address generator circuit **comprises** a finite state machine" is not met by the DMA device 384 and the state machine 385 of Yasuki.

3. The Examiner has omitted one or more elements needed to make a *prima facie* rejection.

With respect to claims 21 and 22, the Office Action mailed July 1, 2005⁵ and the Office Action mailed January 12, 2006⁶

³ See page 2, lines 11-15 of the Advisory Action mailed April 4, 2006, emphasis added.

⁴ See MPEP §2111.03; Mars Inc. v. H.J. HeinzCo., 71 USPQ2d 1837, 1843 (Fed. Cir. 2004); Faber, Robert C., Landis on Mechanics of Patent Claim Drafting, Fourth Edition, Practising Law Institute, 1997, Section 7, pp. II-8,II-9.

⁵ See page 15, line 20 - page 16, line 13.

⁶ See page 20, lines 1-9.

do not apply the references to each specific element of the specifically claimed limitations. For example, claim 21 recites "The apparatus according to claim 1, wherein said idle after chroma state is further configured to move to any of (i) said luma state, (ii) a BTMP after luma state, (iii) an SPU/VBI state, (iv) said idle after luma state, and (v) said chroma state." Claim 22 recites "The apparatus according to claim 1, wherein said idle after luma state is further configured to move to any of (i) said chroma state, (ii) a BTMP after chroma state, (iii) an SPU/VBI state, (iv) said luma state and (v) said idle after chroma state." The Office Actions do not specifically identify where a BTMP after luma state, an SPU/VBI state and a BTMP after chroma state, as presently claimed, are found in the cited references. See the arguments presented on page 16, line 7 through page 17, line 8 of the Amendment After Final filed March 13, 2006. Furthermore, the Advisory Action mailed April 4, 2006 also fails to specifically point out where in the cited references a BTMP after luma state, an SPU/VBI state and a BTMP after chroma state, as presently claimed, are found.⁷ Furthermore, the Advisory Action does not present any objective evidence or convincing line of reasoning why one of ordinary skill in the art would recognize the voltage levels of signals (as illustrated by timing diagrams, e.g., FIGS. 6A-6L in Yasuki) as being the same as the state of a finite state machine illustrated in a state diagram (e.g., FIG. 27 in the

⁷See page 7, section 5, pages 11-12, section 9 of the Advisory Action mailed April 4, 2006.

specification). Therefore, the Office Action does not appear to meet the Office's burden to establish a factual basis to support a *prima facie* conclusion of obviousness with respect to claims 21 and 22. Therefore, the rejection of claims 21 and 22 do not appear to be sustainable and should be withdrawn.

Applicant's representative believes that clear errors in the Examiner's rejection(s) exist or the Examiner has omitted one or more essential elements needed for a *prima facie* rejection.

The Examiner is respectfully invited to call the Applicant's representative between the hours of 9 a.m. and 5 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller

Registration No. 42,892

Dated: May 10, 2006

c/o Henry Groth
Intellectual Property Law Department
LSI Logic Corporation
1621 Barber Lane
MS: D-106 Legal
Milpitas, CA 95035

Docket No.: 00-323 / 1496.00121